PRO-LOG® CORPORATION

STD 7000

7904 TTL
79C04 CMOS
Decoded I/O Utility Card

USER'S MANUAL

4/84

FOREWORD

This manual explains how to use Pro-Log's 7904 and 79C04 decoded I/O utility cards. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7707. We welcome your suggestions on how we can improve our instructions.

The 7904 and 79C04 are part of Pro-Log's Series 7000 STD BUS hardware. Our products are modular, and they are designed and built with second-sourced parts that are industry standards. They provide the industrial manager with the means of using his own people to control the design, production, and maintenance of the company's products that use STD BUS hardware.

Pro-Log supports its products with thorough and complete documentation. Also, to provide maximum assistance to the user, we teach courses on how to design with, and to use, microprocessors and the STD BUS products.

You may find the following Pro-Log documents useful in your work: the **Microprocessor User's Guide** and the **Series 7000 STD BUS Technical Manual**. If you would like a copy of these publications, please submit your request on your company letterhead.

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REFERENCES/BIBLIOGRAPHY

The following are publications which further explain the STD BUS, microprocessor methodology, and HCMOS logic characteristics.

Microprocessor User's Guide, Pro-Log Corporation.

Series 7000 STD BUS Technical Manual, Pro-Log Corporation.

Motorola High Speed CMOS Logic Data, DL 129 Series A (First Ed.), Technical Information Center, Austin, TX (Motorola, 1983). (See section 4.)

QMOS High Speed Logic, Somerville, NJ (RCA, 1982).

Wakeman, Larry, **AN-317 AC Characteristics of HCMOS**, (Application Note), National Semiconductor Corporation, Sept., 1982.

SECTION 1
Purpose and Main Features

PURPOSE

The 7904 and 79C04 are printed circuit cards designed for prototyping I/O circuitry. They provide complete STD BUS buffering and I/O port select decoding. They also provide access to the upper eight bits of the address bus, the control bus, and the power bus. A 4.0 by 4.3-inch (101.6 by 109.2 mm) grid of holes on 0.1-inch (2.54 mm) centers is provided for adding components. These plated-through holes accommodate 0.025-inch (0.64 mm) square wirewrap posts.

The 79C04 is fully implemented in CMOS to offer a high degree of noise immunity, low power consumption, and a wide temperature range.

FEATURES

- Data bus buffers with hysteresis
- Decodes 8 sequential addresses for input ports
- Decodes 8 sequential addresses for output ports
- Access to all STD BUS signals and power buses
- Plated-through holes accommodate 0.025-inch (0.64 mm) square posts
- 17.2 square inches (111 cm^2) of breadboard area
- Processor independent

ADDITIONAL FEATURES of 79C04

- High speed CMOS
- High noise immunity
- Low power consumption
- Wide temperature range

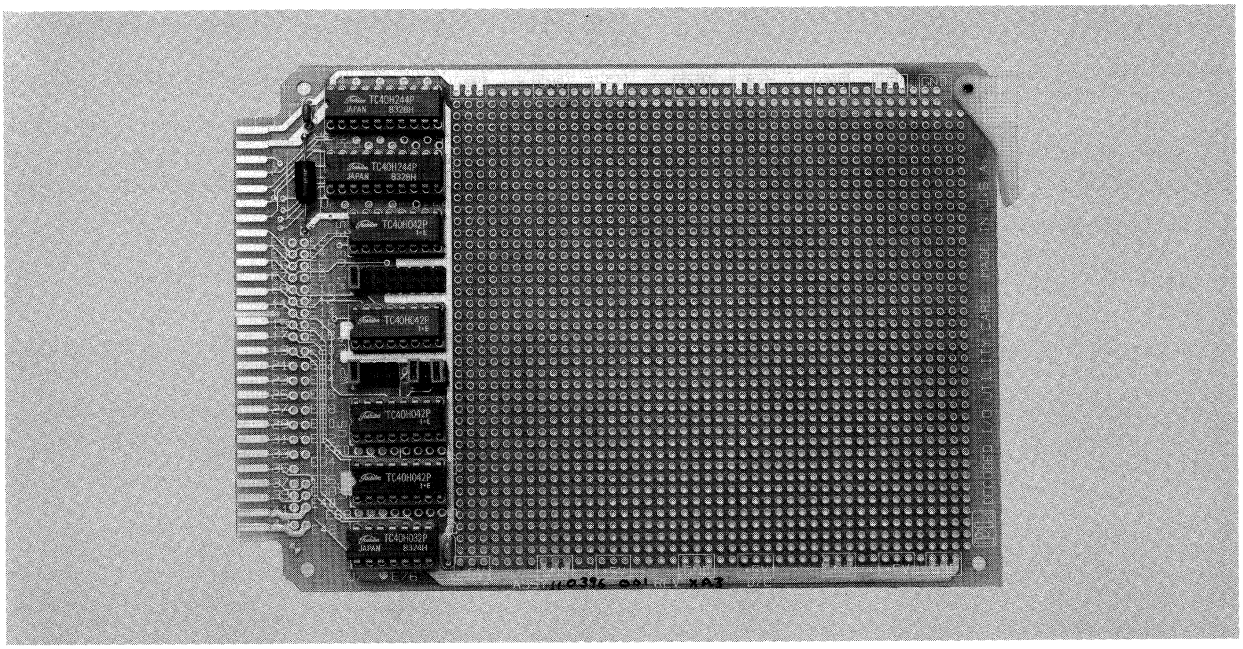


Figure 1-1. 7904/79C04 Decoder I/O Utility Card

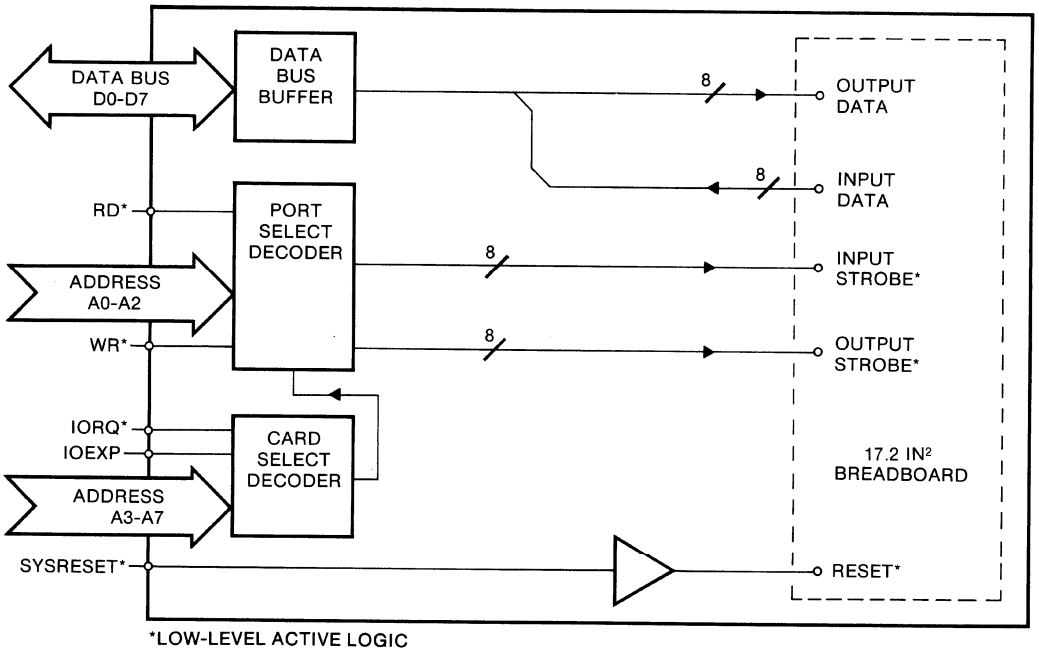


Figure 1-2. 7904/79C04 Block Diagram

FUNCTIONAL DESCRIPTION

The following describes each block in the block diagram (figure 1-2).

Data Bus Buffers — two octal buffers, one for inputs and one for outputs, provide buffering and direction control of the data bus.

Card Select Decoder — two 4- to 10-line decoders decode A_3 to A_7 address lines, IORQ* and IOEXP*. A card select signal occurs when the active decoded line matches the jumper location.

Port Select Decoders — two 4- to 10-line decoders decode A_0 to A_2 address lines and RD* or WR* line to activate one of eight input port select lines (IS0-IS7), or one of eight output port select lines (OS0-OS7).

SYSRESET* Buffer — provides a means for resetting I/O latches. The signal is buffered to connect to devices in the breadboard area without overloading the STD BUS SYSRESET* line.

Breadboard Area — provides a location for prototype circuits. It consists of a 4.0- by 4.3-inch grid of plated-through holes on 0.1-inch centers.

STD address and control buses are available at plated-through holes. Heavy power and ground traces along each long edge of the card are connected to plated-through holes adjacent to the breadboard area.

The breadboard area is compatible with both wire-wrapping and insulation-displacement wiring methods.

LOCATION OF SIGNIFICANT FEATURES

Figure 1-3 shows the locations of significant features of 7904 and 79C04 cards.

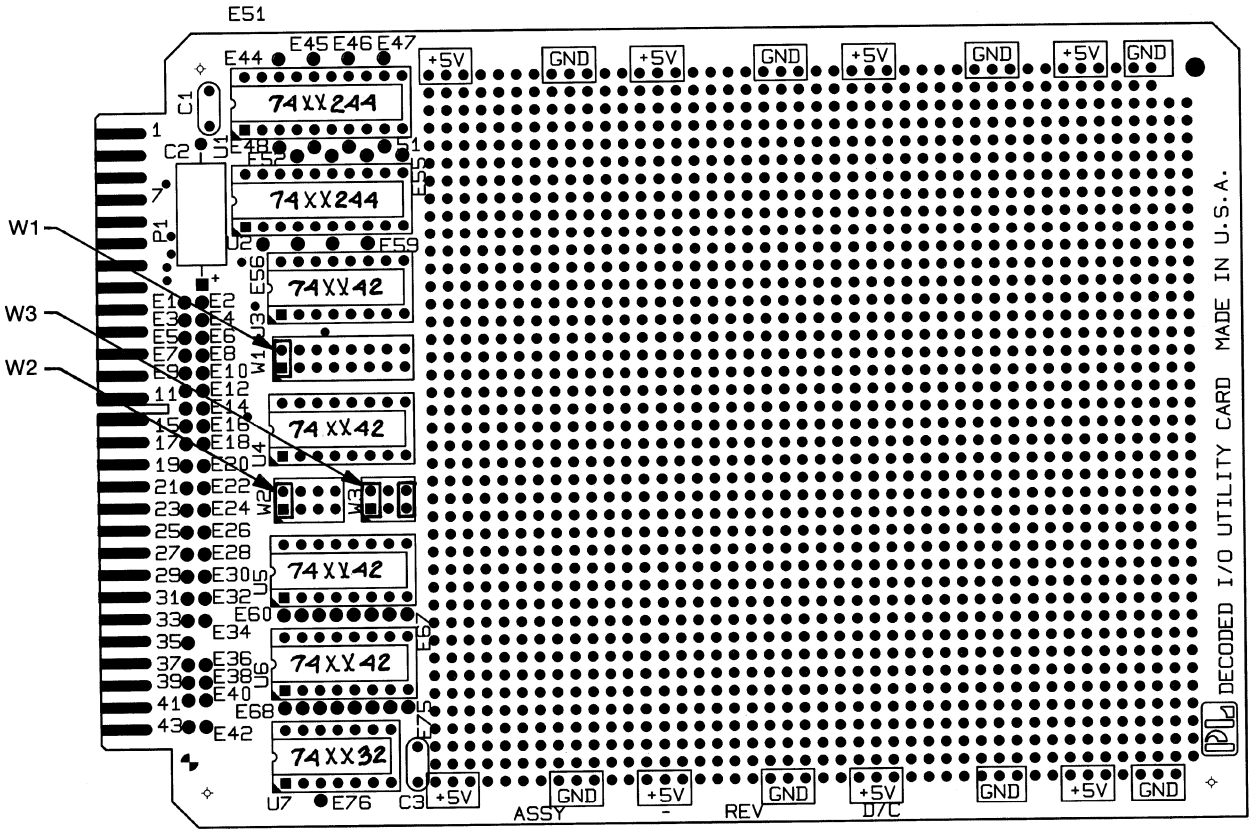


Figure 1-3. Significant Features (7904/79C04)

SECTION 2
Installation and Specifications

INSTALLATION

CAUTION

To prevent possible damage to your STD BUS system, make sure power is **off** before inserting a card into the card rack or removing a card from the card rack.

With the card ejector toward the top, insert the 7904 or 79C04 into any slot in the card rack. See figure 2-1. Empty slots on one or both sides of the card may be required if tall components or long wirewrap pins are used in the breadboard area.

To access the card, install it in either end of an open-ended card rack (card ejector toward the top) or use a Pro-Log 7901 card extender. Plug the 7901 into any slot in the card rack and plug the 7904 or 79C04 into the connector on the card extender.

The 79C04 is designed to operate in CMOS logic level STD systems, while the 7904 is designed for conventional LSTTL logic level systems.

CAUTION

All unconnected pins of CMOS devices must be protected from electrostatic discharge; therefore, all card connector pins must be connected together or the card enclosed in a conductive plastic bag when it is not installed in the rack.

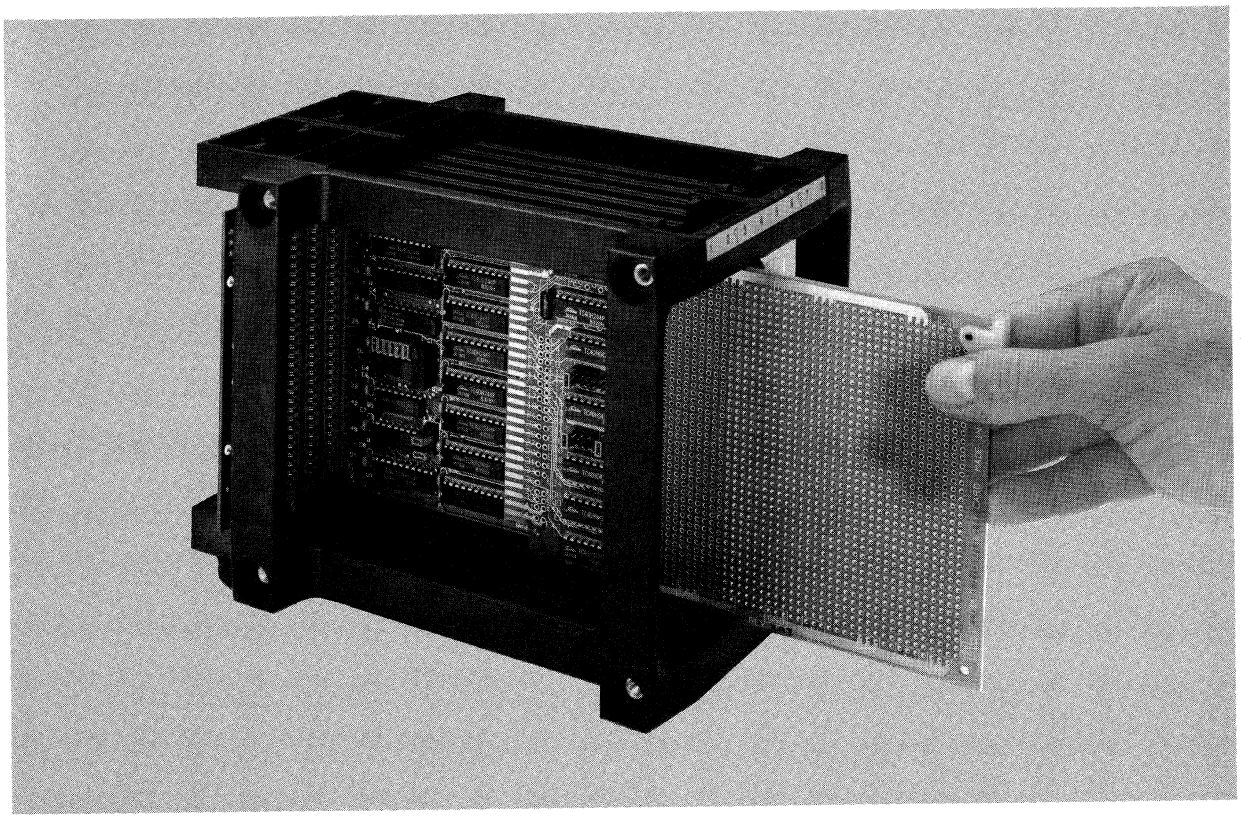


Figure 2-1. Installation (7904/79C04)

ADDRESS REMAPPING

The 7904 and 79C04 each occupy eight addresses. As shipped, they are mapped at addresses 00 to 07. The card(s) can be remapped to any eight consecutive addresses from 00 to FF by moving jumpers W1 and W2. The first of the eight addresses must be a hex number divisible by eight. Figure 2-2 (page 2-4) shows W1 and W2 jumper locations for all eight-address blocks available. Only one jumper is to be placed on each of these headers for any configuration.

TERMINATION AND LOADING

A termination network is not required for Pro-Log's CMOS STD BUS systems. (In fact, using Pro-Log's 7909A terminator card in a CMOS STD system will degrade the system performance as a result of its capacitive loading.)

Since the input impedance of CMOS is very large, the main restriction on fanout is load capacitance. As the total capacitive load on an output is increased, the propagation delays increase, along with power consumption. Since Pro-Log's 24-slot 7106 motherboard uses terminatino that presents large capacitive loads, it should not be used with CMOS cards. Check any other termination in the system for capacitive loading and power dissipation.

ALTERNATE DATA BUS BUFFER SELECTION

Header W3 provides a means for selecting the data bus buffers with alternate circuitry. See schematic, figures 5-1 and 5-2 (pages 5-2 through 5-5). The input buffer (U2) can be permanently selected by connecting its Select line to ground with a jumper between pins 4 and 6 of W3. Output buffer U1 can similarly be selected by placing a jumper between pins 1 and 3 of W3. The buffers can also be controlled by the user's logic by removing the jumpers and making wirewrap connections from the user's logic to header W3, pins 1 and 6.

ADDR	JUMPERS
00	W1: 1-2* W2: 1-2*
01	
02	
03	
04	
05	
06	
07	
08	W1: 1-2 W2: 3-4
09	
0A	
0B	
0C	
0D	
0E	
0F	
10	W1: 1-2 W2: 5-6
11	
12	
13	
14	
15	
16	
17	
18	W1: 1-2 W2: 7-8
19	
1A	
1B	
1C	
1D	
1E	
1F	
20	W1: 3-4 W2: 1-2
21	
22	
23	
24	
25	
26	
27	
28	W1: 3-4 W2: 3-4
29	
2A	
2B	
2C	
2D	
2E	
2F	
30	W1: 3-4 W2: 5-6
31	
32	
33	
34	
35	
36	
37	
38	W1: 3-4 W2: 7-8
39	
3A	
3B	
3C	
3D	
3E	
3F	

ADDR	JUMPERS
40	W1: 5-6 W2: 1-2
41	
42	
43	
44	
45	
46	
47	
48	W1: 5-6 W2: 3-4
49	
4A	
4B	
4C	
4D	
4E	
4F	
50	W1: 5-6 W1: 5-6
51	
52	
53	
54	
55	
56	
57	
58	W1: 5-6 W2: 7-8
59	
5A	
5B	
5C	
5D	
5E	
5F	
60	W1: 7-8 W2: 1-2
61	
62	
63	
64	
65	
66	
67	
68	W1: 7-8 W2: 3-4
69	
6A	
6B	
6C	
6D	
6E	
6F	
70	W1: 7-8 W2: 5-6
71	
72	
73	
74	
75	
76	
77	
78	W1: 7-8 W2: 7-8
79	
7A	
7B	
7C	
7D	
7E	
7F	

ADDR	JUMPERS
80	W1: 9-10 W2: 1-2
81	
82	
83	
84	
85	
86	
87	
88	W1: 9-10 W2: 3-4
89	
8A	
8B	
8C	
8D	
8E	
8F	
90	W1: 9-10 W1: 5-6
91	
92	
93	
94	
95	
96	
97	
98	W1: 9-10 W2: 7-8
99	
9A	
9B	
9C	
9D	
9E	
9F	
A0	W1: 11-12 W2: 1-2
A1	
A2	
A3	
A4	
A5	
A6	
A7	
A8	W1: 11-12 W2: 3-4
A9	
AA	
AB	
AC	
AD	
AE	
AF	
B0	W1: 11-12 W2: 5-6
B1	
B2	
B3	
B4	
B5	
B6	
B7	
B8	W1: 11-12 W2: 7-8
B9	
BA	
BB	
BC	
BD	
BE	
BF	

ADDR	JUMPERS
C0	W1: 13-14 W2: 1-2
C1	
C2	
C3	
C4	
C5	
C6	
C7	
C8	W1: 13-14 W2: 3-4
C9	
CA	
CB	
CC	
CD	
CE	
CF	
D0	W1: 13-14 W2: 5-6
D1	
D2	
D3	
D4	
D5	
D6	
D7	
D8	W1: 13-14 W2: 7-8
D9	
DA	
DB	
DC	
DD	
DE	
DF	
E0	W1: 15-16 W2: 1-2
E1	
E2	
E3	
E4	
E5	
E6	
E7	
E8	W1: 15-16 W2: 3-4
E9	
EA	
EB	
EC	
ED	
EE	
EF	
F0	W1: 15-16 W2: 5-6
F1	
F2	
F3	
F4	
F5	
F6	
F7	
F8	W1: 15-16 W2: 7-8
F9	
FA	
FB	
FC	
FD	
FE	
FF	

Figure 2-2. Port Address Mapping (7904/79C04)

SPECIFICATIONS

Electrical

7904

MNEM.	PARAMETER	Recommended Operating Limits			Absolute Nonoperating Limits		UNITS
		MIN	TYP	MAX	MIN	MAX	
Vcc	Supply Voltage	4.75	5.00	5.25	0	7.00	Volts

79C04

MNEM.	PARAMETER	Recommended Operating Limits[1]			Absolute Nonoperating Limits		UNITS
		MIN	TYP	MAX	MIN	MAX	
Vcc	Supply Voltage	4.50	5.00	5.50	0	7.00	Volts

[1] For TTL interfacing, supply voltage must be 5±0.25V.

Figure 2-3. Electrical Specifications (7904/79C04)

Environmental

7904

PARAMETER	Recommended Operating Limits			Absolute Nonoperating Limits		UNITS
	MIN	TYP	MAX	MIN	MAX	
Free Air Temperature	0	+25	+65	-40	+75	°C
Humidity	5	—	95[1]	5	95[1]	%RH

79C04

PARAMETER	Recommended Operating Limits			Absolute Nonoperating Limits		UNITS
	MIN	TYP	MAX	MIN	MAX	
Free Air Temperature	40	+25	+85	-40	+100	°C
Humidity	5	—	95[1]	5	95[1]	%RH

[1] Noncondensing

Figure 2-4. Environmental Specifications (7904/79C04)

Supply Current

7904

MNEM.	PARAMETER	OPERATING LIMITS			UNITS
		MIN	TYP	MAX	
Icc	Vcc Supply Current	—	92	162	mA

79C04

MNEM.	PARAMETER	OPERATING LIMITS[1] [2]			UNITS
		MIN	TYP	MAX	
Icc	Vcc Supply Current	—	0.02	0.2	mA

[1] Quiescent value with all inputs at Vcc or GND.
[2] Supply current for logic provided. Add user circuitry supply current.

Figure 2-5. Supply Current Over Operating Range (7904/79C04)

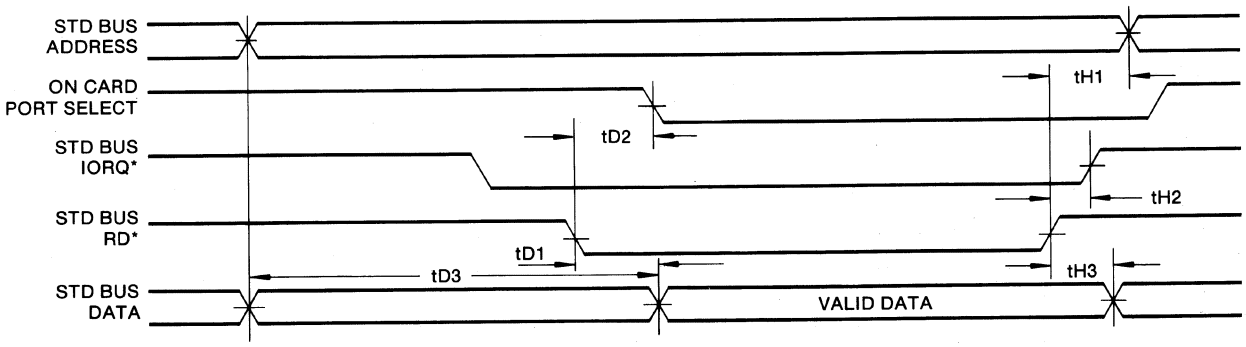
Mechanical

The 7904 and 79C04 meet all general STD mechanical specifications.

TIMING

7904 and 79C04 STD BUS timing is shown in figures 2-6 and 2-7. In each figure, the signal is shown with the implied condition that all other signals are valid before the signal becomes valid. Timing data is exclusive of circuitry added by the user. These timing diagrams are independent of CPU card timing, but must be compared with the CPU card timing to ensure that the 7904 or 79C04 decoding and your breadboarded logic can respond to the CPU in the time allowed for I/O operations.

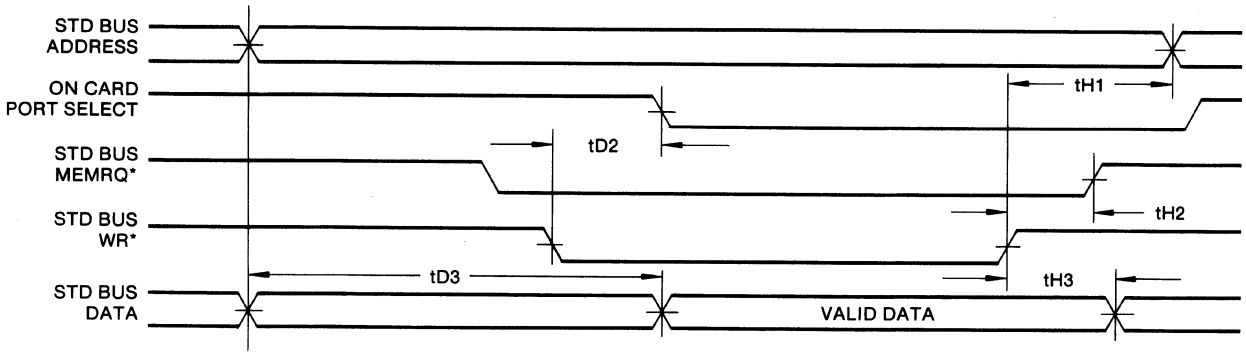
All times given are in nanoseconds. Timing given is for the entire operating supply voltage and temperature ranges.



SYMBOL	PARAMETER	7904		79C04	
		MIN	MAX	MIN	MAX
tD1	Data delay from RD* active		62		146
tD2	Port select active from RD* active		62		116
tD3	Data delay from Address		134		282
tH1	Address hold after RD* inactive	50		179	
tH2	IORQ* hold after RD* inactive	50		179	
tH3	Data hold after RD* inactive	0		150	

All times given in nanoseconds.

Figure 2-6. Input Timing



SYMBOL	PARAMETER	7904		79C04	
		MIN	MAX	MIN	MAX
tD1	Data delay from WR* active		62		146
tD2	Port select active from WR* active		62		116
tD3	Data delay from Address		134		282
tH1	Address hold after WR* inactive	50		179	
tH2	IORQ* hold after WR* inactive	50			
tH3	Data hold after WR* inactive	0		150	

All times given in nanoseconds.

Figure 2-7. Output Timing

STD INTERFACE

Figures 2-8 and 2-9 show the STD pinout, loading and drive presented by the 7904 and 79C04.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	VCC		+5V	1		VCC	+5V
4	GND		GROUND	3		GND	GROUND
6			-5V	5			-5V
8	1	55	D7	7	55	1	D3
10	1	55	D6	9	55	1	D2
12	1	55	D5	11	55	1	D1
14	1	55	D4	13	55	1	D0
16			A15	15		1	A7
18			A14	17		1	A6
20			A13	19		1	A5
22			A12	21		1	A4
24			A11	23		1	A3
26			A10	25		2	A2
28			A9	27		2	A1
30			A8	29		2	A0
32	1		RD*	31		1	WR*
34			MEMRQ*	33		1	IORQ*
36			MEMEX	35		1	IOEXP
38			MCSYNC*	37			REFRESH*
40			STATUS 0*	39			STATUS 1*
42			BUSRQ*	41			BUSAK*
44			INTRQ*	43			INTAK*
46			NMIRQ*	45			WAITRQ*
48			PBRESET*	47		1	SYSRESET*
50			CNTRL*	49			CLOCK*
52	IN		PCI	51	OUT		PCO
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

* Low-level active logic

Figure 2-8. STD Edge Connector (7904)

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
2	IN		+5V	1		IN	+5V
4	IN		GROUND	3		IN	GROUND
6			-5V	5			-5V
8	1	20	D7	7	20	1	D3
10	1	20	D6	9	20	1	D2
12	1	20	D5	11	20	1	D1
14			D4	13		1	D0
16			A15	15		1	A7
18			A14	17		1	A6
20			A13	19		1	A5
22			A12	21		1	A4
24			A11	23		1	A3
26			A10	25		2	A2
28			A9	27		2	A1
30			A8	29		2	A0
32	1		RD*	31		1	WR*
34			MEMRQ*	33		1	IORQ*
36			MEMEX	35		1	IOEXP
38			MCSYNC*	37			REFRESH*
40			STATUS 0*	39			STATUS 1*
42			BUSRQ*	41			BUSAK*
44			INTRQ*	43			INTAK*
46			NMIRQ*	45			WAITRQ*
48			PBRESET*	47		1	SYSRESET*
50			CNTRL*	49			CLOCK*
52	IN		PCI	51		OUT	PCO
54			AUX GND	53			AUX GND
56			AUX -V	55			AUX +V

[1] CMOS LOAD = pF at ±5 μA

* Low-level active logic

Figure 2-9. STD Edge Connector (79C04)

SECTION 3
Operation and Programming

INTRODUCTION

The operation of these cards can best be explained by describing a specific application. As explained earlier, each card can be used for as many as eight input and eight output ports; however, the application chosen is one using two input and two output ports.

APPLICATION EXAMPLE

Specification

The following application example shows how to design and build a card with the following functions:

- One-digit, seven-segment readout at address 25H
- One 8-bit, latched output port at address 23H
- Two 8-bit, buffered input ports at addresses 21H and 25H
- One I/O connector for connection to the input and output lines
- SYSRESET* used for clearing the output port and the readout

Refer to figure 3-1 for a block diagram of this circuit.

Port Address Mapping

Refer to figure 2-2 (page 2-3) to determine where the W1 and W2 jumpers must be placed to map the ports to the specified addresses. All specified addresses are within a block of eight. The block is 20H to 27H and the figure shows that W1 must be at 3-4 and W2 at 1-2.

Referring to the schematic in figure 5-1 (page 5-2) it is evident that, with the card mapped from 20 to 27, output port select lines OS3* (E71) and OS5* (E73) from U6 must be used for the output ports 23H and 25H, and input port select lines IS1* (E61) and IS5* (E65) from U5 must be used for input ports 21H and 25H.

The output port select lines are connected to the Clock inputs of the output latches and the input port select lines are connected to the Enable lines of the input buffers.

The four output lines from output port 25H are connected to the inputs of the BCD to the 7-segment decoder/driver, and the 7-output lines from this are in turn connected to the 7-segment display.

SYSRESET* (E76) is connected to the Clear inputs of each of the output latches. All incoming data lines (E44 through E51) are connected to the data input lines of output latch 2; the four lower ones (E44 through E47) are connected to the four input lines used on output latch 1. All outgoing data lines (E52 through E59) are connected to the eight input lines of each of the input buffers.

All the lines from output port 25H and input ports 21H and 25H are connected to the I/O connector.

The output port select lines are connected to the Clock inputs of the output latches and the input port select lines are connected to the Enable lines of the input buffers.

The four output lines from output port 25H are connected to the inputs of the BCD to the 7-segment decoder/driver, and the 7-output lines from this are in turn connected to the 7-segment display.

SYSRESET* (E76) is connected to the Clear inputs of each of the output latches. All incoming data lines (E44 through E51) are connected to the data input lines of output latch 2; the four lower ones (E44 through E47) are connected to the four input lines used on output latch 1. All outgoing data lines (E52 through E59) are connected to the eight input lines of each of the input buffers.

All the lines from output port 25H and input ports 21H and 25H are connected to the I/O connector.

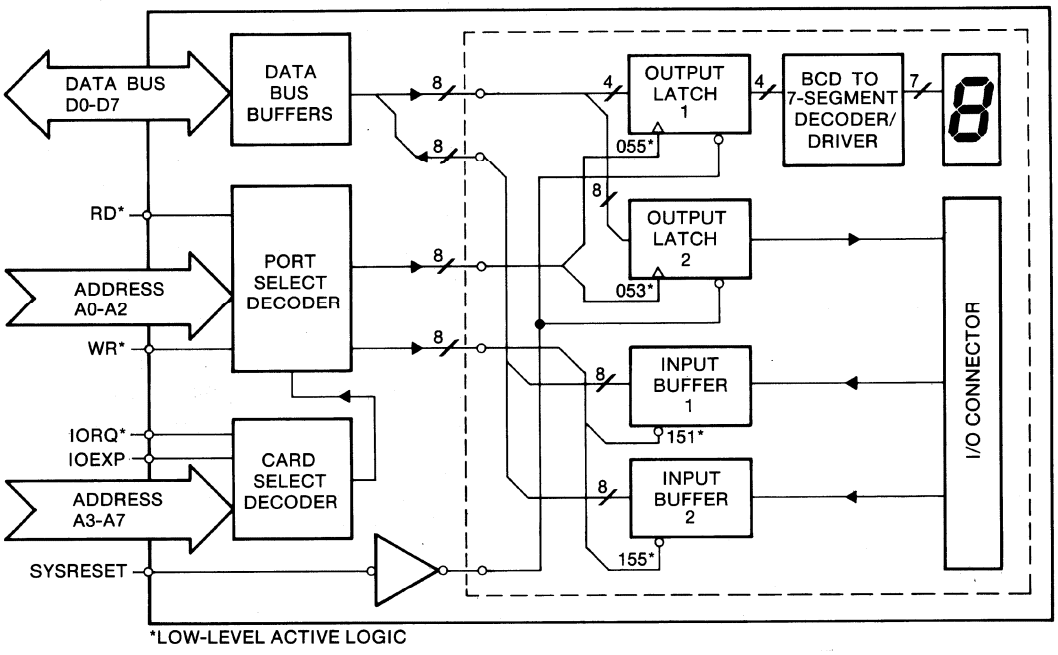


Figure 3-1. Application Example Block Diagram

Hardware

The hardware required to support this application is:

- One 7904 STD card
- Two 8-bit buffers
- Two 8-bit latches (one may be 4-bit)
- One BCD to 7-segment decoder/driver
- One 7-segment readout
- One 24-pin connector
- Four 0.01 microfarads ceramic bypass capacitors
- IC sockets as required

Construction

Two recommended breadboard techniques are wire wrapping and insulation displacement. The latter may be obtained from the 3M Company.

All connections to the existing circuits are made through the pads labeled E1 through E75. Wires may be soldered directly to these pads or individual posts for wirewrap or insulation displacement may be soldered into these pads.

Figure 3-2 is an illustration of a proposed layout. Four 0.01 microfarad capacitors are placed between VCC and Ground for noise decoupling.

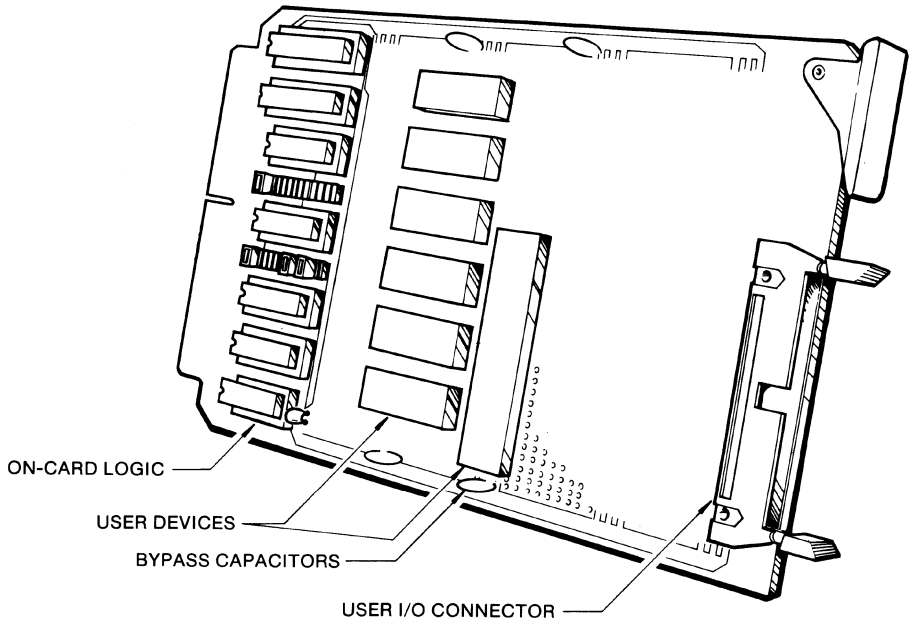


Figure 3-2. Construction Example (7904/79C04)

SECTION 4
Operating Software

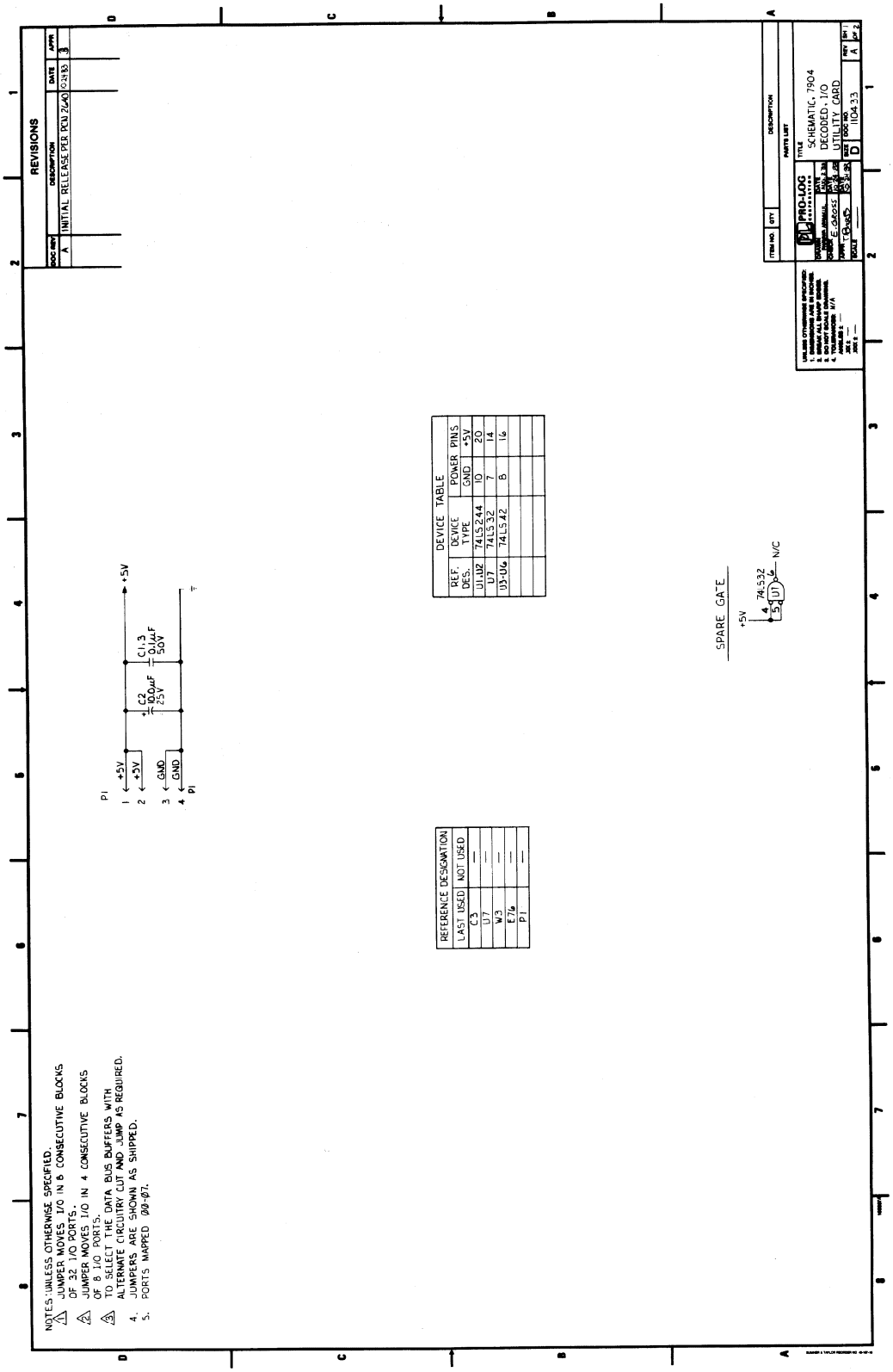
This section is normally reserved for software. The 7904 and 79C04 require no special software.

SECTION 5
Maintenance

REFERENCE DRAWINGS

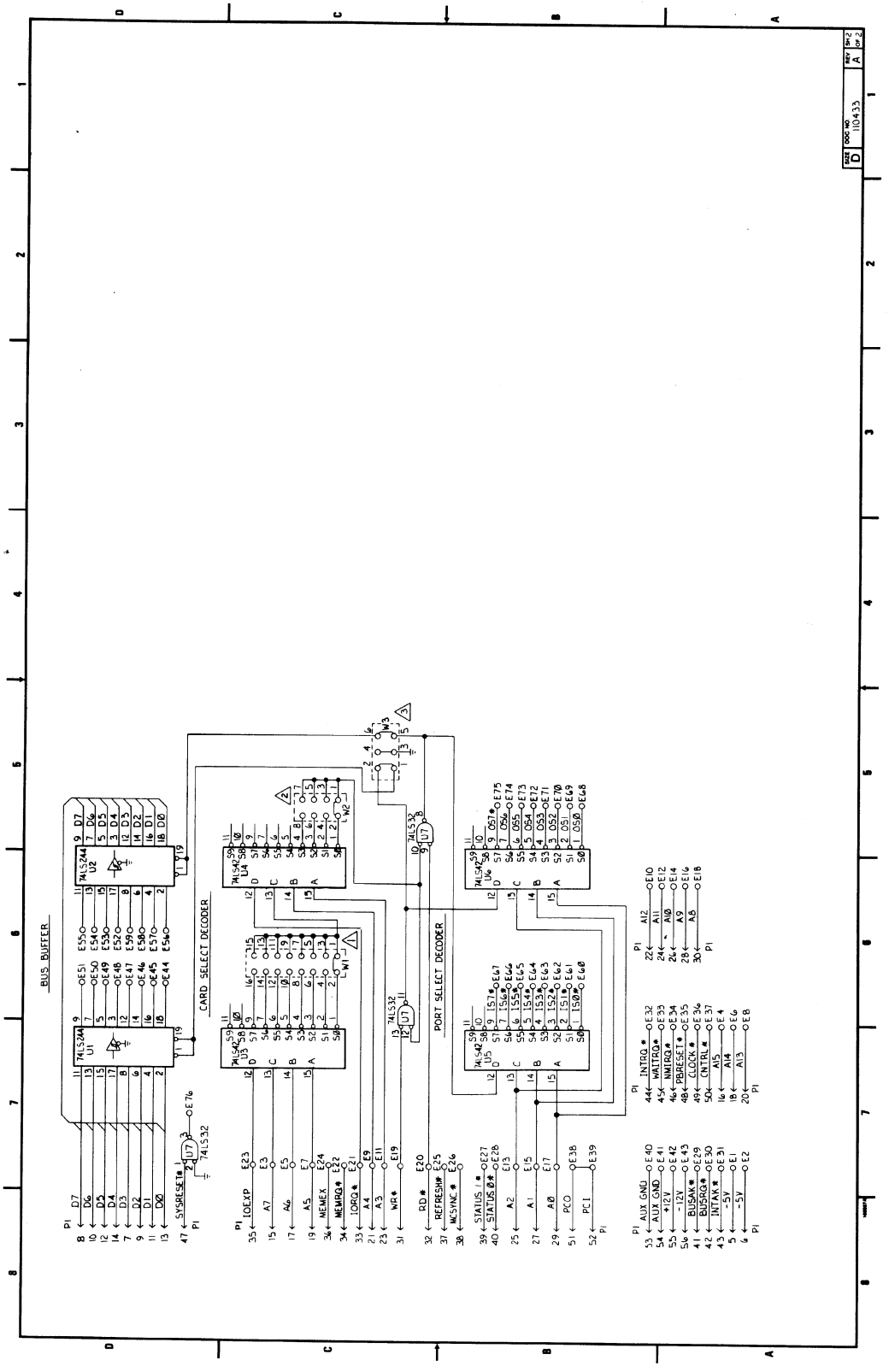
The schematics (figures 5-1 and 5-2) and assembly drawings (figures 5-3 and 5-4) in the following pages are included in this manual for **REFERENCE ONLY**. Because improvements may have been made to the card(s) since this manual was published, they may differ in some respects from the card and documentation the user received from Pro-Log.

The schematic and assembly drawing shipped by Pro-Log with the card are those from which the card was manufactured.



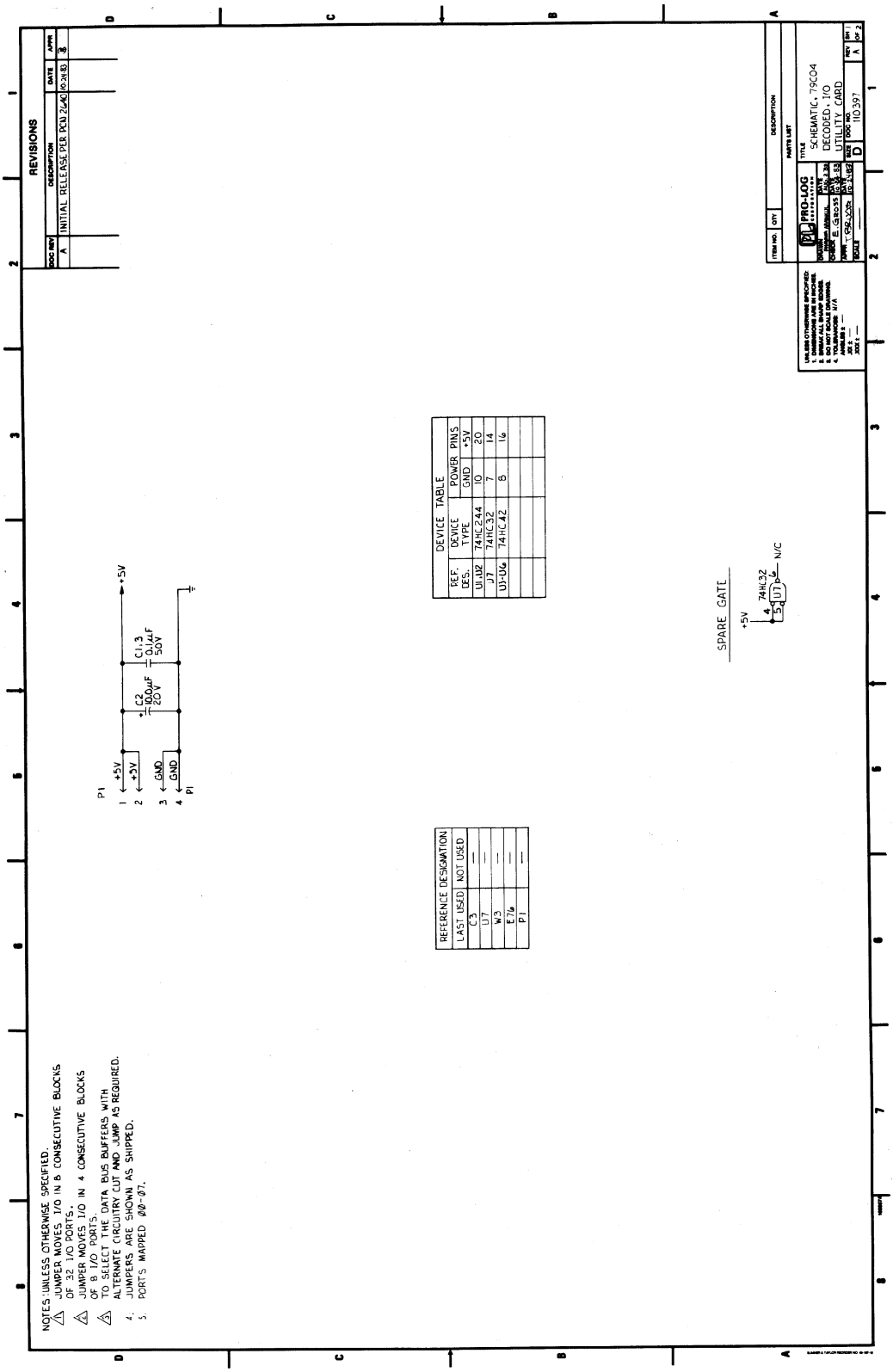
(Reference only. See documents shipped with the card.)

Figure 5-1. 7904 Schematic Page 1



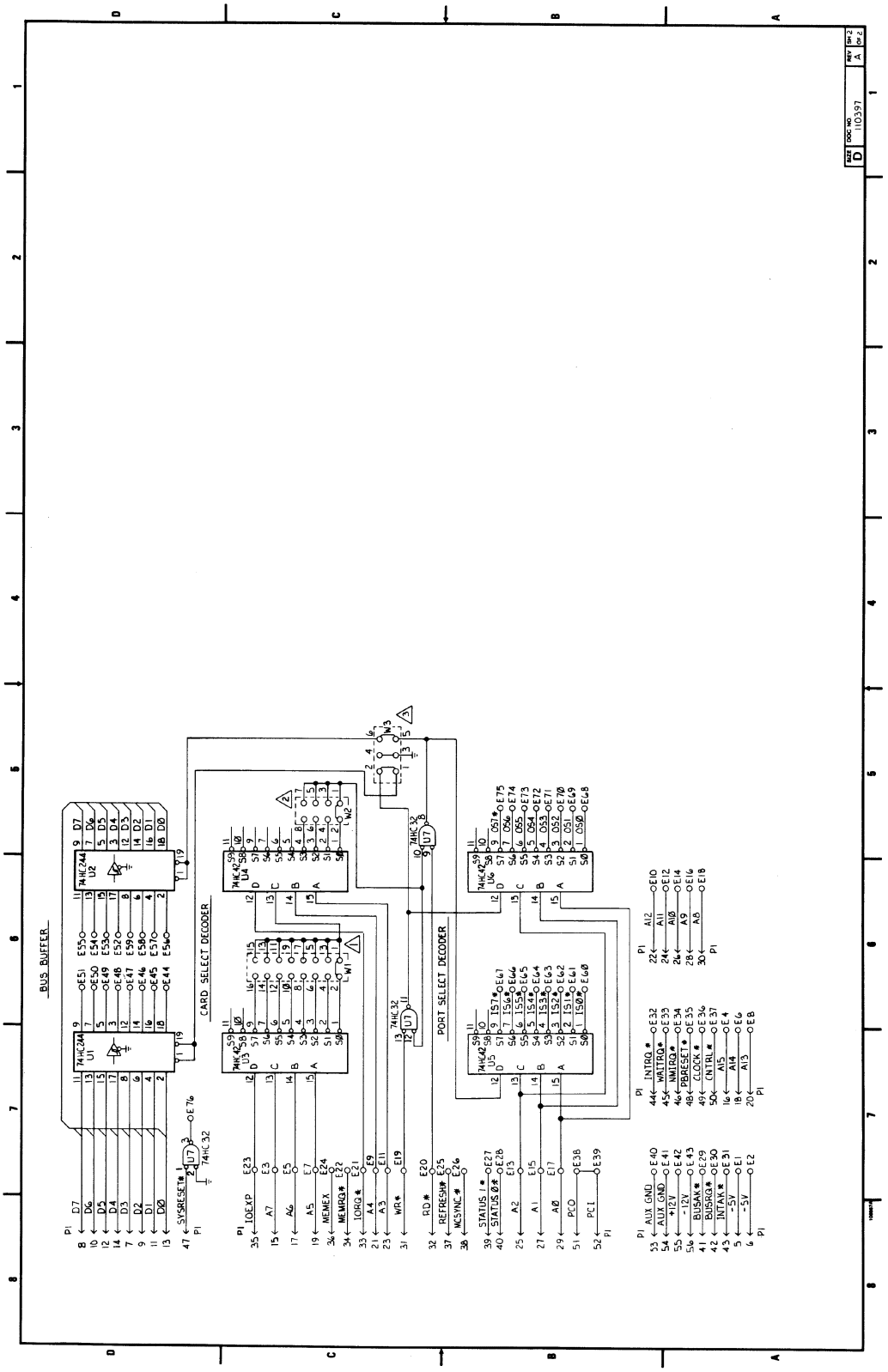
(Reference only. See documents shipped with the card.)

Figure 5-1. 7904 Schematic (continued)



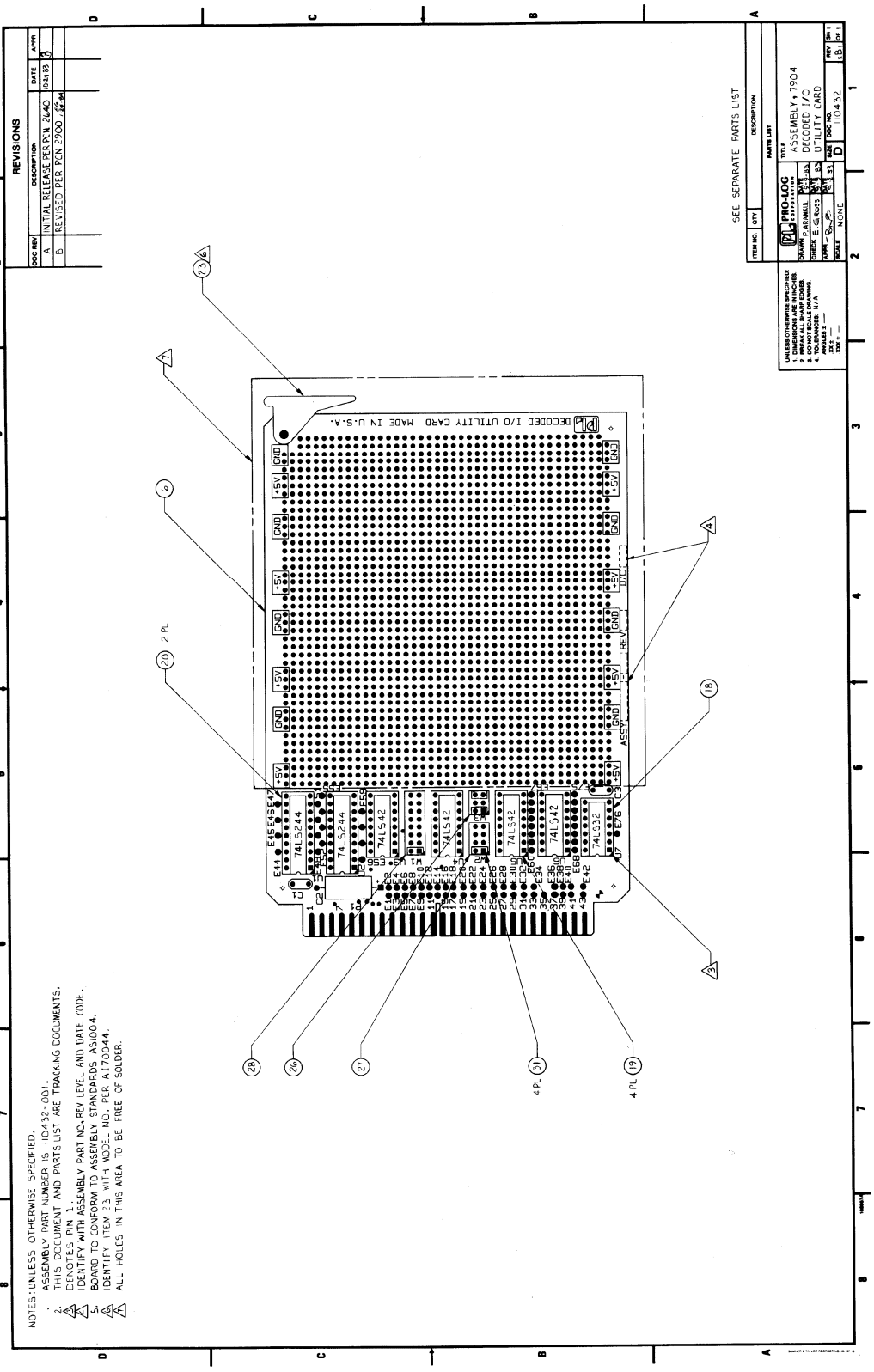
(Reference only. See documents shipped with the card.)

Figure 5-2. 79C04 Schematic



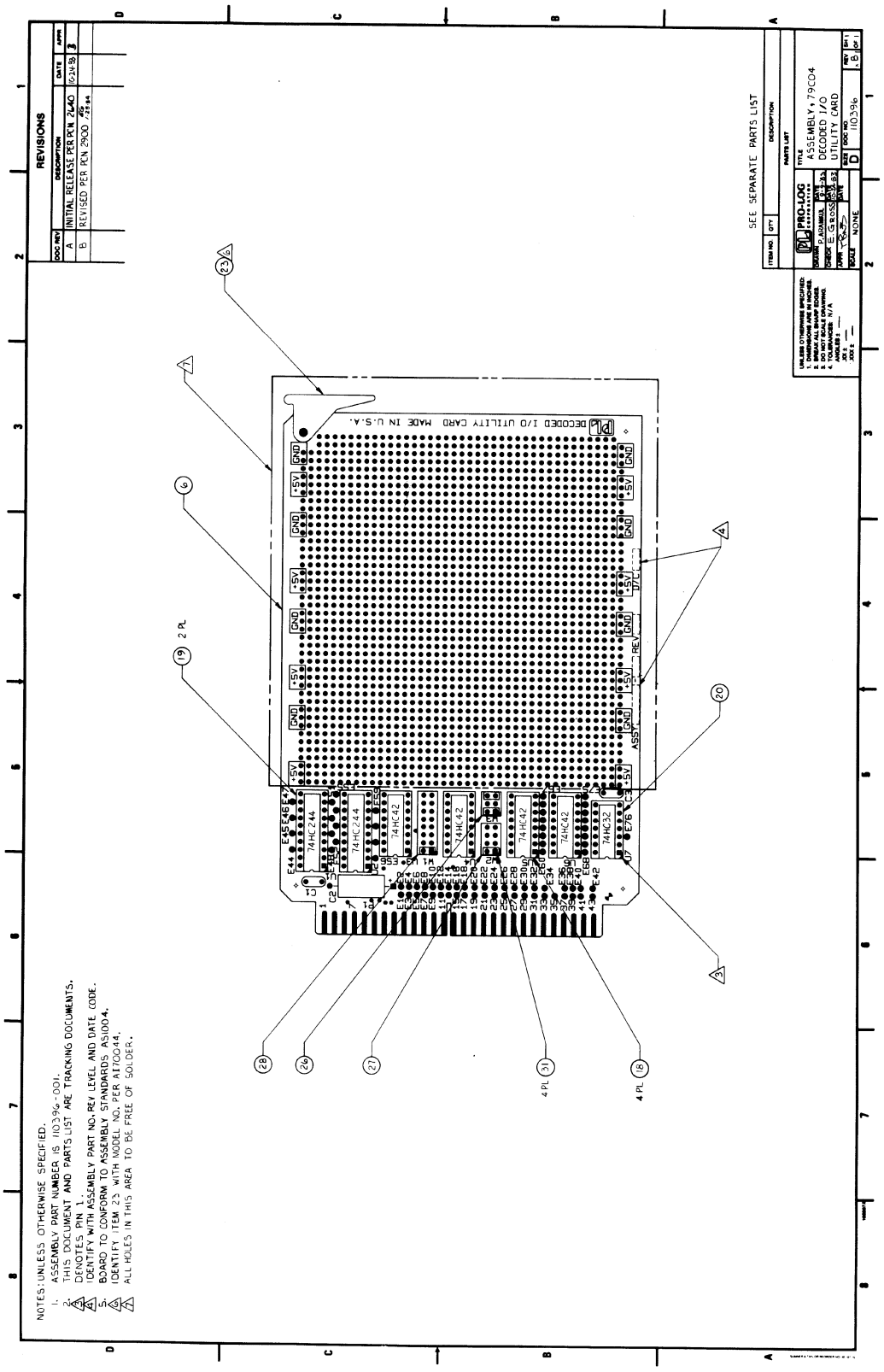
(Reference only. See documents shipped with the card.)

Figure 5-2. 79C04 Schematic (continued)



(Reference only. See documents shipped with the card.)

Figure 5-3. 7904 Assembly



(Reference only. See documents shipped with the card.)

Figure 5-4. 79C04 Assembly

RETURN FOR REPAIR PROCEDURES

Domestic Customers:

1. Call Customer Support at (800) 538-9570, ext. 3617. In California call (408) 646-3617 from 7 a.m. to 3 p.m. (PST).
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, and reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

CAUTION

Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during handling. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, California 93940

   Reference CRO #_____

International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

Limited Warranty

Limited Warranty: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned f.o.b. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller or the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

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